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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
TOLEDO, FERNANDO L

ART UNIT	PAPER NUMBER
2823	9

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/660,324	Applicant(s) AHN ET AL.	
	Examiner Fernando Toledo	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover she t with th correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *88,90-95 and 97-123* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *88,90-95 and 97-123* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claim 122 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 122 recites the limitation "further comprising the step of processing said insulating layer to produce at least one active circuit element." It is not clear how can an insulating layer may be processed to form an active circuit element. By definition alone, an insulating layer does not conduct electricity and therefore all elements formed with it are passive. One of ordinary skill in the art can form active devices that contain an insulating layer (e.g. transistors). But, by processing an insulating layer by itself will not produce an active device. Is this the same insulating layer that carries the passive circuit element? If not, why the active circuit element not shown in the drawings as it is clear, it is part of the invention? Are both the passive circuit element and the active circuit element formed in the same insulating layer? Is the passive circuit element the same as the active circuit element?

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 88, 90 – 95, 97 – 100, 105 – 118 and 123 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stone (U. S. patent 5,770,476) in view of Yamazaki (U. S. patent 6,002,161).

In re claim 88, Stone discloses in the U. S. patent 5,770,476; figures 1 – 3 and related text, a process for forming an interposer layer element 100, including the steps of; providing an insulating layer 7; processing the insulating layer to produce at least one passive circuit element 17 on or within the insulating layer; bonding an integrated circuit chip 31 to the interposer layer 100 such that the integrated circuit chip is electrically connected to the passive circuit element (figure 2); forming a pattern on or within the insulating layer, the metallization pattern 21 connected with the passive circuit element 17 (figure 1).

Stone dose not show wherein the insulating layer is provided on at least one silicon substrate; wherein the passive circuit element is being separated from the silicon substrate by a portion of the insulating layer; and a portion of the insulating layer having a thickness such that the passive circuit element is electrically shielded from the silicon substrate.

However, Yamazaki in the U. S. patent 6,002,161; figures 1 – 15, shows a passive circuit element 11 (i.e. inductor) in an insulating layer 101 that is on at least one surface of a silicon substrate 100 wherein a portion of the insulating layer has a

thickness such that the passive element is electrically shielded from the substrate (column 9).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to form the interposer element of Stone with the teachings of Yamazaki (i.e. shows forming a passive circuit element 11 in an insulating layer 101 that is on at least one surface of a silicon substrate 100 wherein a portion of the insulating layer has a thickness such that the passive element is electrically shielded from the substrate) because in order for a passive element to work it *must* be on an insulating layer, to isolate the passive element from the active elements in the device and Yamazaki will enable the practitioners of Stone to form an interposer layer within an insulating layer in a silicon substrate.

In re claim 90, Stone teaches wherein the step of bonding comprises solder bonding 35 (figure 2).

In re claim 91, Stone teaches wherein the step of bonding comprises flip-chip bonding (figure 2).

In re claim 92, Stone teaches that the insulating layer is formed of an oxide (column 5).

In re claim 93, Stone substantially teaches the invention as claimed, but fails to explicitly teaches that the oxide is SiO_2.

However, silicon dioxide is a notoriously well-known insulating layer that can be readily grown from a silicon substrate. Examiner respectfully submits that Applicant did not contest this assertion therefore, it is considered to be well known in the art.

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have silicon dioxide as the oxide layer in Stone's invention because it is readily grown and choosing a material for its disclosed intended purposes requires only ordinary skill in the art. Note that the specification contains no disclosure of either the critical nature of the claimed material being of silicon oxide or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen material or upon another variable recited in a claim, the Applicant must show that the chosen material is critical. *In re Woodruf*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

In re claim 94, Stone substantially teaches the invention as claimed, but fails to show that the insulating layer has a thickness within a range of three to five microns.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the insulating layer of a thickness of three to five microns, since insulating layer thickness are well known processing variable and it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233. Also, note that the specification contains no disclosure of either the critical nature of the claimed thickness or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen thickness or upon another variable recited in a claim, the Applicant must show that the chosen thickness are critical. *In re Woodruf*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

In re claim 95, Stone substantially teaches wherein the insulating layer includes polimydes among other suitable materials in the invention as claimed but fails to teaches that the insulating layer is formed of polyamide.

However, polyamides have been known in the art to be attractive materials to use as insulating materials because of their high temperature tolerance, they are free of pinholes and cracks, among other advantages. Examiner respectfully submits that Applicant did not contest this assertion, therefore, it is understood that this assertion is considered prior art.

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a polyamide film as an insulating layer because it offers high temperature tolerance and are free of pinholes and cracks among other advantages. Note also that the specification contains no disclosure of either the critical nature of the claimed material being of polymide or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen material or upon another variable recited in a claim, the Applicant must show that the chosen material is critical. *In re Woodruf*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990). Also, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a polymide as an insulating material, since it has been held to be within the general skill of a worker in the art to select a known material on the base of its suitability, for its intended use involves only ordinary skill in the art. *In re Leshin*, 125 USPQ 416.

In re claim 97, Stone teaches wherein the step of processing the insulating layer further comprises the step of producing several passive circuit elements on or within the insulating layer (column 6).

In re claim 98, Stone teaches that the passive circuit element is a resistor element (column 6).

In re claim 99, Stone teaches that the resistor is a thin film resistor (column 6).

In re claim 100, Stone teaches that the passive circuit element includes a capacitor element (column 6).

In re claim 105, Stone teaches that the passive circuit element includes an inductor element (column 6).

In re claim 106, Stone does not explicitly show that the inductor element is a spiral inductor.

However, Yamazaki teaches forming an inductor in a spiral conformation because the inductance properties of an inductor are directly related to the number of turns and hence it must be in a spiral conformation (column 1).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the inductor of Yamazaki in Stone's invention because the practitioners of Stone can form the inductor with Yamazaki's teaching and as evidenced by Yamazaki the inductance properties of an inductor are directly related to the number of turns and hence it must be in a spiral conformation (column 1). The selection of a known inductor pattern on the basis of its suitability for its disclose intended purposes requires only ordinary skill in the art.

In re claim 107, Stone substantially teaches the claimed invention, but fails to show fabricating the passive circuit device for use in RF communication systems.

Since, Stone does form passive electrical devices, therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to use Stone's invention in an RF communications system since it hold similar elements to that the Applicant is claiming.

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to form an RF communication system out of Stone's invention since it is well known in the art that FR communication system have the same elements as those on Stone's invention.

In re claim 108, Stone does not explicitly teach forming a circuitry to use in RF communication systems.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use Stone's invention for RF communication system since the invention is to be used for devices that uses interposers with at least one passive circuit element (column 1).

In re claims 109 and 110, Stone substantially discloses the claimed invention but fails to show wherein at least one passive device is for use in an amplifier (e.g. load or broad band).

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to use one of the passive devices in Stone's invention since it is well known in the art to use inductors as amplifiers.

In re claims 111 and 112, Stone substantially discloses the claimed invention but fails to show that wherein at least one passive circuit device is for use in an oscillator (e.g. control voltage oscillator).

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to use Stone's invention wherein at least one of the passive circuit device is used as an oscillator since it is well known that passive circuit device are used for that purpose.

In re claims 113 – 116, Stone discloses that the integrated circuit chip 31 is used in electronic devices.

Stone does not show that the electronic devices are analog circuitry, digital circuitry, microprocessor and memory chip.

However it is well known to someone having ordinary skill in art, that an electronic device comprises analog circuitry, digital circuitry, microprocessor, memory chip, etc. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the electronic devices of Stone as analog circuitry, digital circuitry, microprocessor and memory chip since analog circuitry, digital circuitry, microprocessor and memory chip are well known in the art. The selection of a known electronic device on the basis of its suitability for the disclosed intended purposes requires only ordinary skill in the art.

In re claim 117, Stone discloses the step of forming a bonding layer, the bonding layer located in the area between the integrated circuit chip and the insulating layer (column 8).

In re claim 118, Stone discloses that the bonding agent is a conductive adhesive among other suitable material (column 8).

Stone does not show that is an epoxy.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to make the conductive adhesive out of epoxy since it has been well known in the art that conductive adhesives are conventionally made out of epoxies.

In re claim 123, Stone discloses providing at least one passive circuit element in each area of the insulating layer, dividing the substrate into areas and bonding at least one integrated circuit chip to each of the areas of the insulating layer to from respective chip carriers (column 1).

3. Claims 101 – 104 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stone and Yamazaki as applied to claims 89 – 100 above, and further in view of Farooq et al. (U. S. patent 5,912,044).

In re claim 101, Stone in view of Yamazaki does not teach that the capacitor is a thin film capacitor.

However, Farooq in the U. S. patent 5,912,044; figures 1 – 8 and related text, discloses a method of forming a thin film capacitor that are to be used typically in interposer layers because the signal propagation characteristics of interposer layers can be further enhanced by placing thin film capacitors (column 1).

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to form a thin film capacitor as taught by Farooq as the

capacitor taught by Stone because it will enable the practitioners of Stone to form the capacitor and by forming a thin film capacitor they will enhance the signal propagation of the device.

In re claim 102, Stone in view of Yamazaki does not teach that the thin film capacitor includes a dielectric layer.

However, Farooq teaches that the thin film capacitor includes a dielectric layer 16 (column 3).

In re claim 103, Stone in view of Yamazaki does not teach that the dielectric layer of the capacitor is an oxide.

However, Farooq teaches that the dielectric 16 can be made of oxides (column 4).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the dielectric film out of an oxide, since it has been held to be within the general skill of a worker in the art to select a known material on the base of its suitability, for its intended use involves only ordinary skill in the art. *In re Leshin*, 125 USPQ 416.

In re claim 104, Stone in view of Yamazaki does not teach that the dielectric film can be formed of oxide-nitride-oxide films.

However, Farooq teaches that the dielectric 16 of the thin-film capacitor can be made of oxide-nitride-oxide films (column 4).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the dielectric film out of an oxide-nitride-oxide film, since it

has been held to be within the general skill of a worker in the art to select a known material on the base of its suitability, for its intended use involves only ordinary skill in the art. *In re Leshin*, 125 USPQ 416.

4. Claims 119 – 121 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stone and Yamazaki as applied to claims 88 – 100 and 105 - 118 above, and further in view of Solberg (U. S. patent 6,121,676).

In re claim 119, Stone shows forming a package out of the interposer element and at least one integrated circuit.

Stone in view of Yamazaki does not teach encapsulating the interposer element and the integrated circuit and having conducting leads on an outer side of the package.

However, Solberg in the U. S. patent 6,121,676; figures 1 – 19 and related text discloses a method of encapsulating an interposer element with at least one integrated circuit (column 8), the package having conducting leads on an outer side of the package to connect to a circuit board.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to encapsulate the package of Stone in view of Yamazaki as taught by Solberg because the teachings of Solberg will enable the practitioners of Stone in view of Yamazaki to form the package as taught by Solberg and therefore realize the function of the device by connecting it to a circuit board.

In re claim 120, Stone in view of Yamazaki do not explicitly show providing conductive leads connecting the interposer element and at least one integrated circuit to the conductive package leads of the circuit package.

However, Solberg teaches forming conductive leads 22 to the package in order to connect the circuit package to a circuit board.

In re claim 121, Stone shows providing an insulating layer to both surfaces of the substrate (figure 1).

Response to Arguments

5. Applicant's arguments filed 23 January 2002 have been fully considered but they are not persuasive for the foregoing reasons.

6. Applicant contests that claim 122 is enabled because it is possible to form an active device with an insulating layer.

Examiner respectfully submits that active devices have insulating layers (e.g. gate oxide of an electrode), however, the limitation of claim 122 claims, processing the insulating layer to produce at least one active circuit element. This can be interpreted that the insulating layer by itself will produce the active circuit element. Office personnel are to give claims their broadest reasonable interpretation in light of the supporting disclosure. In re Morris, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See *also In re Zletz, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) ("During patent examination the pending claims must be interpreted as broadly as their terms reasonably allow. . . . The reason is simply that during patent prosecution when claims can be amended, ambiguities should be recognized, scope and breadth of language explored, and clarification imposed. . . . An essential purpose of patent

examination is to fashion claims that are precise, clear, correct, and unambiguous. Only in this way can uncertainties of claim scope be removed, as much as possible, during the administrative process.").

7. Applicant contests that claim 88 is not anticipated by Stone in view of Yamazaki. Applicant argues:

> However, nowhere within the Stone reference, and certainly not within Figure 2, does Stone disclose an integrated circuit chip being electrically connected to a passive circuit element formed within an interposer layer, as claimed.

Examiner respectfully submits that passive circuit element **17** is electrically connected to circuit chips **31** and **33** via the solder balls **35** and plating material **13** which in turn is electrically connected to conductive plane **21** that connects to passive circuit element **17** as shown in figure 2. Therefore, the passive device of Stone is electrically connected to the circuit chips as shown in figure 2.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fernando Toledo whose telephone number is (703) 305-0567. The examiner can normally be reached on Monday – Friday, 8am – 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

	Fernando Toledo Patent Examiner Art Unit 2823

ft
October 13, 2000

SUPERVISORY PRIMARY EXAMINER
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